IN THE CLAIMS:

Claims 1-34 (Canceled)

35. (currently amended) A COder/DECoder (CODEC) that converts an inbound analog signal to inbound packetized digital data and that converts outbound packetized digital data to an outbound analog signal, the CODEC comprising:

a transcoder having an outbound portion that is operable to convert the outbound packetized digital data to outbound streamed digital data and an inbound portion that is operable to convert inbound streamed digital data to the inbound packetized digital data;

a Digital to Analog Converter (DAC) coupled to the transcoder that is operable to convert the outbound streamed digital data to the outbound analog signal; and

an Analog to Digital Converter (ADC) coupled to the transcoder that is operable to convert the inbound analog signal to the inbound streamed digital data, wherein the ADC includes:

a modulator that is operable to receive the inbound analog signal and a feedback signal and to modulate the analog signal based upon the feedback signal to produce a modulated signal;

a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and

a time dither clock reduction circuit that is operable to produce the feedback signal by applying both clock reduction and time dithering to the modulated signal.

~~a time dither clock reduction circuit that is operable to use both clock reduction and time dithering in an analog to digital conversion process.~~

36. (currently amended) The CODEC of claim 35, wherein the CODEC services a wireless device. ~~the ADC comprises:~~

~~a modulator that is operable to modulate the inbound analog signal to produce a modulated signal at a modulator clock rate;~~

~~a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and~~

~~wherein the time dither clock reduction circuit is operable to receive the modulated signal and to provide the feedback signal to the modulator by applying both clock reduction and time dithering to the modulated signal to produce the feedback signal.~~

37. (currently amended) The CODEC of claim 35 ~~36~~, wherein:

the modulator comprises an analog delta sigma block having an integrator and a quantizer;

the integrator is operable to receive the inbound analog signal and the feedback signal and to produce an integrator output; and

the quantizer is operable to receive the integrator output and to produce the modulated signal.

38. (previously presented) The CODEC of claim 35, wherein the CODEC operates upon audio information.

39. (currently amended) The CODEC of claim 35, wherein the decimation filter comprises at least one integrator, at least one decimator, and at least one digital filter.

~~the ADC comprises:~~

~~a modulator that is operable to receive the inbound analog signal and a feedback signal and to modulate the inbound analog signal to produce a modulated signal at a modulator clock rate;~~

~~a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and~~

~~wherein the time dither clock reduction circuit is operable to receive the modulated signal and to provide the feedback signal to the modulator, wherein the time dither clock reduction circuit is operable to apply both the clock reduction and the time dithering to the modulated signal to produce the feedback signal.~~

40. (currently amended) The CODEC of claim 35 ~~39~~, wherein: the CODEC services a battery powered, hand-held device.

~~the modulator comprises an analog delta sigma block having an integrator and a quantizer;~~

~~the integrator is operable to receive the inbound analog signal and the feedback signal and to produce an integrator output; and~~

~~the quantizer is operable to receive the integrator output and to produce the modulated signal.~~

41. (previously presented) The CODEC of claim 35, wherein the transcoder implements at least one of A-law coding/decoding operations, μ-law coding/decoding operations, and Continuous Variable Slope Delta (CVSD) coding/decoding operations.

42. (currently amended) A wireless network device comprising:

an antenna;

a radio transceiver coupled to the antenna;

a baseband processor coupled to the radio transceiver; and

a COder/DECoder (CODEC) coupled to the baseband processor that is operable to convert an inbound analog signal to inbound packetized digital data and to convert outbound packetized digital data to an outbound analog signal, the CODEC comprising:

a transcoder having an outbound portion that is operable to convert the outbound packetized digital data to outbound streamed digital data and an inbound portion that is operable to convert inbound streamed digital data to the inbound packetized digital data;

a Digital to Analog Converter (DAC) coupled to the transcoder that is operable to convert the outbound streamed digital data to the outbound analog signal; and

an Analog to Digital Converter (ADC) coupled to the transcoder that is operable to convert the inbound analog signal to the inbound streamed digital data, wherein the ADC includes:

a modulator that is operable to receive the inbound analog signal and a feedback signal and to modulate the analog signal to produce a modulated signal;

a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and

a time dither clock reduction circuit that is operable to produce the feedback signal by applying both clock reduction and time dithering to the modulated signal.

~~a time dither clock reduction circuit that is operable to use both clock reduction and time dithering in an analog to digital conversion process.~~

43. (currently amended) The wireless network device of claim 42, wherein the radio transceiver supports Wireless Personal Area Network communications. ~~ADC of the CODEC comprises:~~

~~a modulator that is operable to modulate the inbound analog signal to produce a modulated signal at a modulator clock rate;~~

~~a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and~~

~~wherein the time dither clock reduction circuit is operable to receive the modulated signal and to provide the feedback signal to the modulator by applying both clock reduction and time dithering to the modulated signal to produce the feedback signal.~~

44. (currently amended) The wireless network device of claim 42 ~~43~~, wherein:

the modulator comprises an analog delta sigma block having an integrator and a quantizer;

the integrator is operable to receive the inbound analog signal and the feedback signal and to produce an integrator output; and

the quantizer is operable to receive the integrator output and to produce the modulated signal.

45. (currently amended) The wireless network device of claim 42, wherein the decimation filter comprises at least one integrator, at least one decimator, and at least one digital filter.

~~the ADC of the CODEC comprises:~~

~~a modulator that is operable to receive the inbound analog signal and a feedback signal and to modulate the inbound analog signal to produce a modulated signal at a modulator clock rate;~~

~~a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and~~

~~wherein the time dither clock reduction circuit is operable to receive the modulated signal and to provide the feedback signal to the modulator, wherein the time dither clock reduction circuit is operable to apply both the clock reduction and the time dithering to the modulated signal to produce the feedback signal.~~

46. (currently amended) The wireless network device of claim 42 ~~45~~, ~~wherein:~~ the wireless network device supports Wireless Local Area Network communications.

~~the modulator comprises an analog delta sigma block having an integrator and a quantizer;~~

~~the integrator is operable to receive the inbound analog signal and the feedback signal and to produce an integrator output; and~~

~~the quantizer is operable to receive the integrator output and to produce the modulated signal.~~

47. (previously presented) The wireless network device of claim 42, wherein the transcoder of the CODEC implements at least one of A-law coding/decoding operations, μ-law coding/decoding operations, and Continuous Variable Slope Delta (CVSD) coding/decoding operations.

48. (currently amended) A wireless headset comprising:

a frame;

an antenna ~~mounted on~~ coupled to the frame;

a radio transceiver coupled to the antenna;

a baseband processor coupled to the radio transceiver;

a COder/DECoder (CODEC) coupled to the baseband processor that is operable to convert an inbound analog signal to inbound packetized digital data and to convert outbound packetized digital data to an outbound analog signal, the CODEC comprising:

a transcoder having an outbound portion that is operable to convert the outbound packetized digital data to outbound streamed digital data and an inbound portion that is operable to convert inbound streamed digital data to the inbound packetized digital data;

a Digital to Analog Converter (DAC) coupled to the transcoder that is operable to convert the outbound streamed digital data to the outbound analog signal; and

an Analog to Digital Converter (ADC) coupled to the transcoder that is operable to convert the inbound analog signal to the inbound streamed digital data, wherein the ADC includes:

a modulator that is operable to receive the inbound analog signal and a feedback signal and to modulate the analog signal to produce a modulated signal;

a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and

a time dither clock reduction circuit that is operable to produce the feedback signal by applying both clock reduction and time dithering to the

modulated signal; ~~a time dither clock reduction circuit that is operable to use both clock reduction and time dithering in an analog to digital conversion process;~~

a speaker coupled to the frame and to the CODEC; and

a microphone coupled to the frame and to the CODEC.

49. (currently amended) The wireless headset of claim 48, wherein the radio transceiver supports Wireless Personal Area Network communications.

~~the ADC of the CODEC comprises:~~

~~a modulator that is operable to modulate the inbound analog signal to produce a modulated signal at a modulator clock rate;~~

~~a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and~~

~~wherein the time dither clock reduction circuit is operable to receive the modulated signal and to provide the feedback signal to the modulator by applying both clock reduction and time dithering to the modulated signal to produce the feedback signal.~~

50. (currently amended) The wireless headset of claim 48 ~~49~~, wherein:

the modulator comprises an analog delta sigma block having an integrator and a quantizer;

the integrator is operable to receive the inbound analog signal and the feedback signal and to produce an integrator output; and

the quantizer is operable to receive the integrator output and to produce the modulated signal.

51. (currently amended) The wireless headset of claim 48 ~~49~~, wherein the decimation filter comprises at least one integrator, at least one decimator, and at least one digital filter.

~~the ADC of the CODEC comprises:~~

~~a modulator that is operable to receive the inbound analog signal and a feedback signal and to modulate the inbound analog signal to produce a modulated signal at a modulator clock rate;~~

~~a decimation filter coupled to the modulator that is operable to receive the modulated signal and to decimate and filter the modulated signal to produce the inbound streamed digital data; and~~

~~wherein the time dither clock reduction circuit is operable to receive the modulated signal and to provide the feedback signal to the modulator, wherein the time dither clock reduction circuit is operable to apply both the clock reduction and the time dithering to the modulated signal to produce the feedback signal.~~

52. (currently amended) The wireless headset of claim 48 ~~51~~, wherein:

the modulator comprises an analog delta sigma block having an integrator and a quantizer;

the integrator is operable to receive the inbound analog signal and the feedback signal and to produce an integrator output; and

the quantizer is operable to receive the integrator output and to produce the modulated signal.

53. (previously presented) The wireless headset of claim 48, wherein the transcoder of the CODEC implements at least one of A-law coding/decoding operations, μ-law coding/decoding operations, and Continuous Variable Slope Delta (CVSD) coding/decoding operations.

54. (previously presented) The wireless headset of claim 48, wherein the radio transceiver supports at least one version of the Bluetooth Specification.